

NISIN

触摸显示模组产品规格承认书

Display Module Specifications for Approval

客户： 客户型号：			NS630FH3002BZ01		
批准 APPROVED	审核 CHECKED	拟制 DESIGNED	批准 APPROVED	审核 CHECKED	拟制 DESIGNED



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1.产品规格 (Product Specifications)

面板类型 (Panel Type)	TFT LCD
面板尺寸 (Panel Size)	6.3 inch
显示类型 (Display Type)	Normal Black
分辨率 (Resolution)	1080 (RGB) x 2340 (dot)
显示点间距 (Dot Pitch)	20.7Um X 60.1Um
显示色彩 (color)	16.7M
视角 (View Angle)	U/D/L/R: 80/80/80/80
显示驱动 IC (Display Driver IC)	FT8719P
接口类型 (Interface Type)	MIPI 4 Lane
触摸类型 (TP Type)	INCELL
触摸 IC (TP IC)	FT8719P
外形尺寸 (Dimensions)	72.56(H) X 156.66(V) X 2.3(T) (mm)
显示区尺寸 (Display area)	67.07 x 145.31 (mm)
模组亮度 (Module Brightness)	450Cd/m ² (MIN) /X:0.29±0.03, Y:0.31±0.03
触摸点数 Touch points	5
触摸按键 Touch Key Number	0
触摸屏固件版本	Version:

3. 接口定义 (The Interface Definition)

4. 电性特性 (Electrical Characteristics)

4.1 ABSOLUTE MAXIMUM RATINGS

7. ELECTRICAL SPECIFICATION

7.1. Absolute Maximum Ratings

(AVDD = 4.5V ~ 6.5V, AVEE = -4.5V ~ -6.5V, VDDI = 1.65V ~ 1.95V, Ta = -30°C ~ 87°C)

Parameter	Symbol	Rating	Unit	Note
Power Supply Voltage 1	VDDI-VSS	-0.3 ~ +1.95	V	
Power Supply Voltage 2	VDDAM-VSS	-0.3 ~ +1.95	V	
Power Supply voltage 4	VDDI_TP-VSS	-0.3 ~ +1.95	V	
Power Supply Voltage 5	AVDD-VSS	-0.3 ~ +6.5	V	
Power Supply Voltage 6	VSS-AVEE	-0.3 ~ +6.5	V	
Power Supply Voltage 7	VGH-VGL	-0.3 ~ +32	V	
Input Voltage	Vt	-0.3 ~ VDDI+0.3	V	
Operating Temperature	Topr	-30 ~ +70	°C	
Storage Temperature	Tstg	-55 ~ +110	°C	

Note1. The maximum applicable voltage on any pin with respect to 0V.

Note2. Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.



4.2 DC CHARACTERISTICS

4.2.1 DC Characteristics for Panel Driving

7.2.1. Basic DC characteristic

(AVDD = 4.5V~6.5V,AVEE = -4.5V~-6.5V,VDDI = 1.65V~1.95V, Ta = -30°C ~ 87°C)

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	AVDD	Operating Voltage	4.5	5.5	6.5	V	
Analog Operating voltage	AVEE	Operating Voltage	-6.5	-5.5	-4.5	V	
Logic Operating voltage	VDDI	I/O supply voltage	1.65	1.8	1.95	V	
Digital Operating voltage	VDD	Digital supply voltage	1.075	1.2	1.5	V	
Hissi interface Operating voltage	VDDAM	MIPI supply voltage	1.65	1.8	1.95	V	
Touch Operating voltage	VDDI_TP	Touch supply voltage	1.65	1.8	1.95	V	
Input / Output							
Logic High level input voltage	VIH	-	0.7*VDDI	-	VDDI	V	
Logic Low level input voltage	VIL	-	VSS	-	0.3*VDDI	V	
Logic High level output voltage	VOH	IOH = -1.0mA	0.8*VDDI	-	VDDI	V	
Logic Low level output voltage	VOL	IOL = +1.0mA	VSS	-	0.2*VDDI	V	
Logic High level input current	I _{IH}	V _{in} = VDDI or VDDAM	-	-	1	uA	
Logic Low level input current	I _{IL}	V _{in} = VDDI or VDDAM	-1	-	-	uA	
VCOM Operation							
VCOMDC output voltage	VCOM	-	-2.4	-	1.2	V	

Source Driver							
Gamma positive reference voltage	VGMP	VGMP<AVDD-0.5V	2.85	-	6.0	V	
Gamma negative reference voltage	VGMN	VGMN>AVEE+0.5V	-6.0	-	-2.85	V	
Source output voltage	VSD	-	VGMN	-	VGMP	-	
Output deviation voltage (Source positive output channel)	V _{dev}	Sout >=+4.2V, Sout <=+0.8V	-	-	30	mV	
		+4.2V>Sout>+0.8V	-	-	20	mV	
Output deviation voltage (Source negative output channel)	V _{dev}	Sout <=-4.2V, Sout >=-0.8V	-	-	30	mV	
		-4.2V<Sout<-0.8V	-	-	20	mV	
Output offset voltage	V _{OFSET}	-	-	-	100	mv	
Reference Voltage							
Internal reference voltage	V _{REF}	-	1.94	2.0	2.06	V	
Internal reference voltage	V _{REF_TP}	-	2	3.5	4.5	V	

Booster operation							
Pump output voltage	VGH	Range=(AVDD-AVEE) ~(3XAVDD-2 AVEE)	5.5	-	18	V	
Pump output voltage	VGL	Range=(AVEE+AVEE) ~(2AVEE-AVDD)	-18.0	-	-5.5	V	
Regulator output voltage	VCL	-	-3	-3	-3.75	V	

Note1. The maximum applicable voltage on any pin with respect to 0V.

Note2. Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

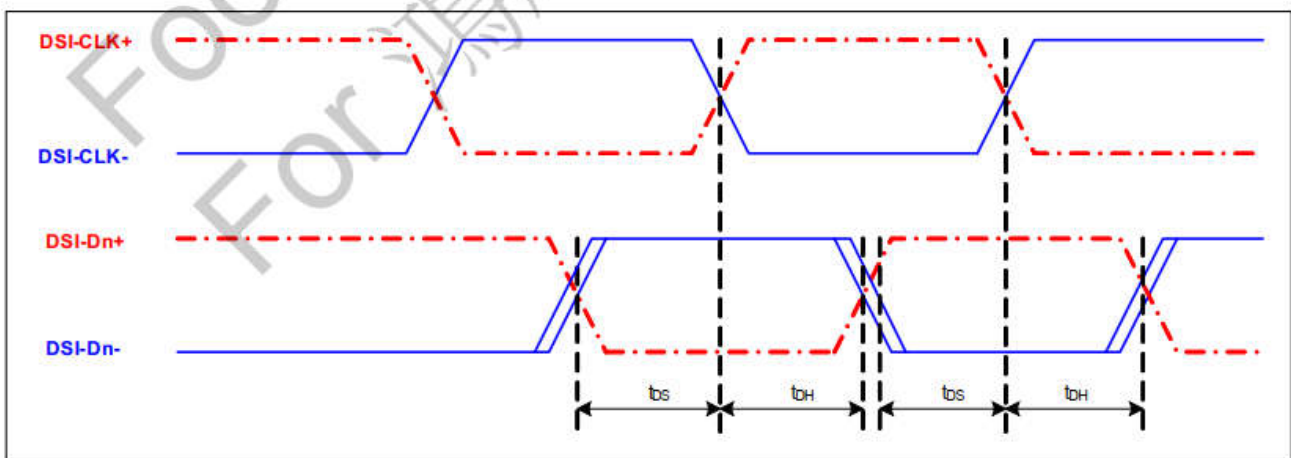
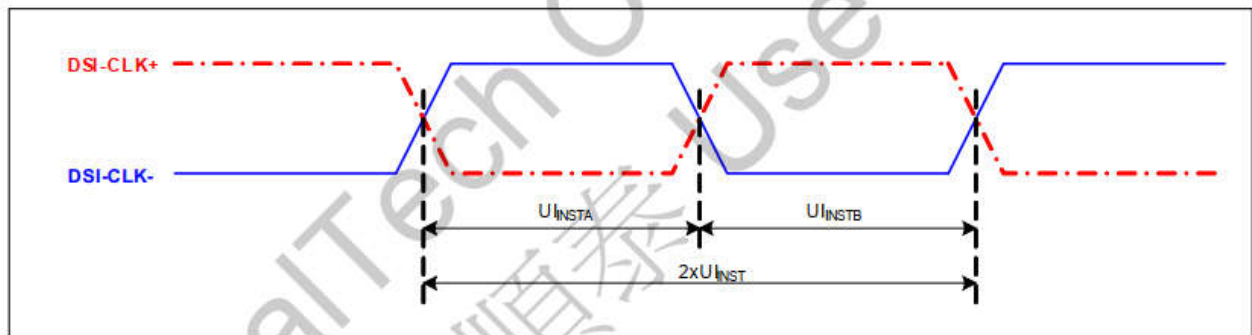
Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Power supply voltage for MIPI Interface						
Power supply voltage for MIPI interface	LVDSVDD	-	1.1	1.2	1.3	V
LPDT Input Characteristics						
Pad signal voltage range	VI	-	-50	-	1350	mV
Ground Shift	VGNSH	-	-50	-	50	mV
Logic 0 input threshold	VIL	-	0	-	550	mV
Logic 1 input threshold	VIH	-	880	-	LVDSVDD	mV
Input hysteresis	VHYST	-	25	-	-	mV
LPDT Output Characteristics						
Output low level	VOL	-	-50	-	50	mV
Output high level	VOH	-	1.1	1.2	1.3	V
Logic 1 contention threshold	VILCD,MIN	-	450	-	LVDSVDD	mV
Logic 0 contention threshold	VIHCD,MAX	-	0	-	200	mV
Output impedance of LPDT	ZOLP	-	80	100	125	ohm
Hi-speed Input/Output Characteristics						
Single-end input low voltage	VILHS	-	-40	-	-	mV
Single-end input high voltage	VIHHS	-	-	-	460	mV
Common mode voltage	VCMRXDC	-	70	-	330	mV
Hi-speed transmit voltage	VOD	-	140	200	250	mV
Differential input impedance	ZID	-	80	100	125	ohm

4.3 AC CHARACTERISTICS

7.3.2. MIPI-DSI characteristics

7.3.2.1. DPHY High speed mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Mode						
DSI-CLK+/-	$2xU_{INST}$	Double UI instantaneous	1.67	-	25	ns
DSI-CLK+/-	U_{INSTA}, U_{INSTB}	UI instantaneous Halfs	0.84	-	12.5	ns
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3UI	ps



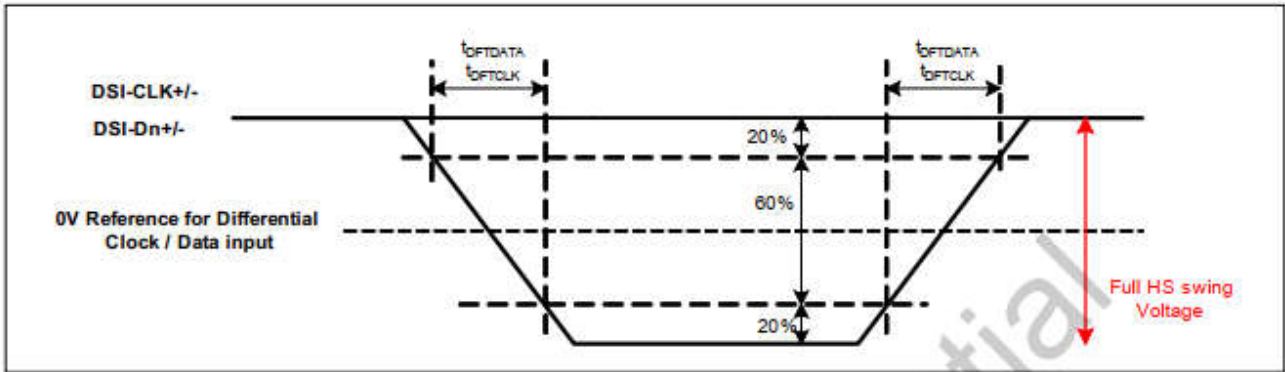


Figure: AC characteristics for MIPI-DSI High speed mode

7.3.2.2. DPHY Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power mode						
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU Display Module	50	-	-	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module MPU	58	-	-	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2XT_{LPXD}$	ns
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	$5XT_{LPXD}$	-	-	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4XT_{LPXD}$	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of T_{LPXM} / T_{LPXD} between MCU and display module	2/3	-	3/2	-

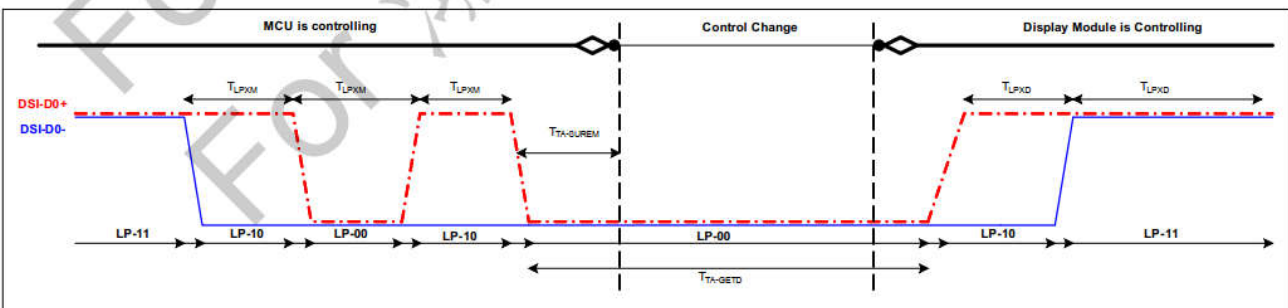


Figure: BTA from the MCU to the Display Module

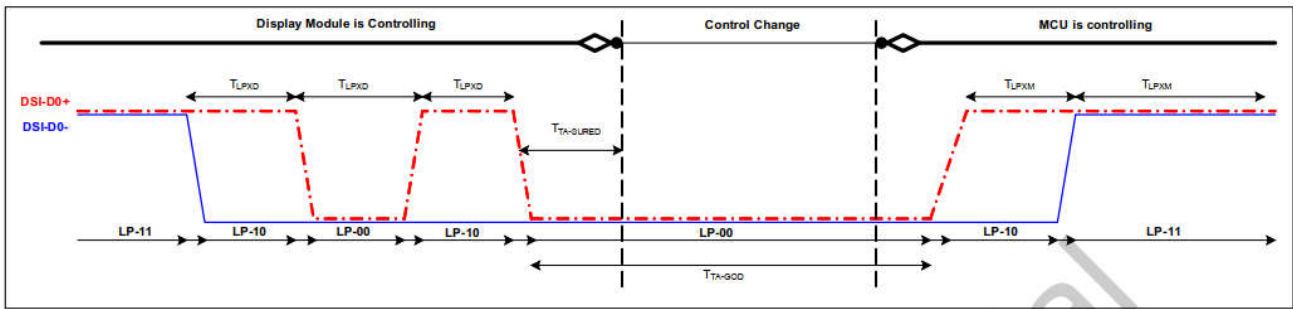


Figure: BTA from the Display Module to the MCU

7.3.2.3. DPHY Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	T_{LPX}	Length of any low-power state period	50	-	-	ns
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4UI	-	85ns + 6UI	ns
DSI-Dn+/-	$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time to drive HS-0 before the sync sequence	145ns + 10UI	-	-	ns
DSI-Dn+/-	$T_{D-TERM-EN}$	Time to enable Data Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	35ns + 4UI	ns
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns + 4UI	ns
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns
DSI-Dn+/-	T_{EoT}	Time from start of $T_{HS-TRAIL}$ period to start of LP-11 state	-	-	105ns + 12UI	ns

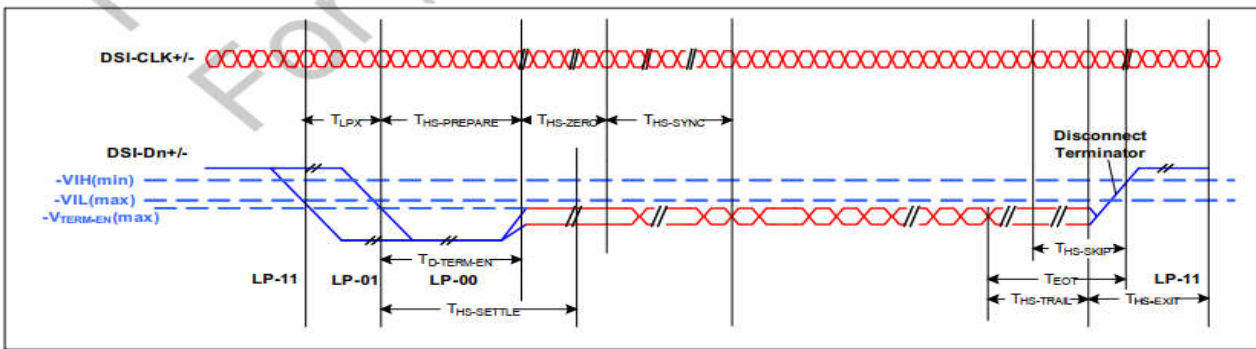


Figure: High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$60ns + 52UI$	-	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time for lead HS-0 drive period before starting Clock	300	-	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	T_{EoT}	Time from start of $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	$105ns + 12UI$	ns

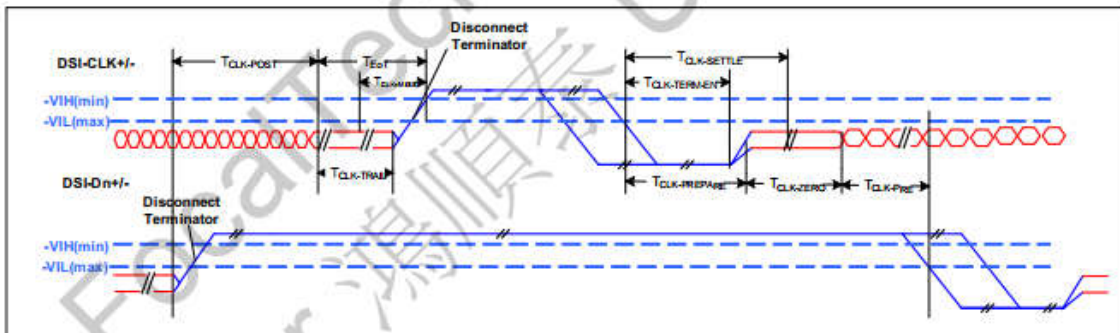
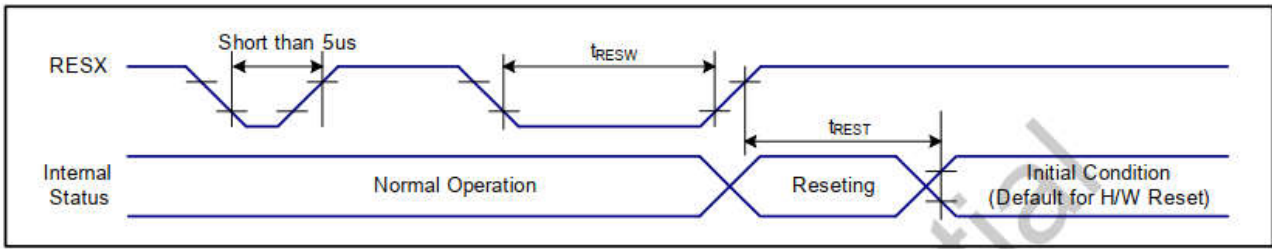


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

7.3. AC characteristic

7.3.1. Reset timing characteristics



VSS=0V, VDDI=1.65V to 3.6V, Ta = -30°C to 70°C

Symbol	Parameter	Related Pin	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	Reset applied during Sleep-in mode	us
			70	-	-	Reset applied during Sleep-out mode	ms
t_{REST}	*2) Reset complete time	-	-	-	10	Reset applied during Sleep-in mode	ms
		-	-	-	120	Reset applied during Sleep-out mode	ms

Table: Reset input timing

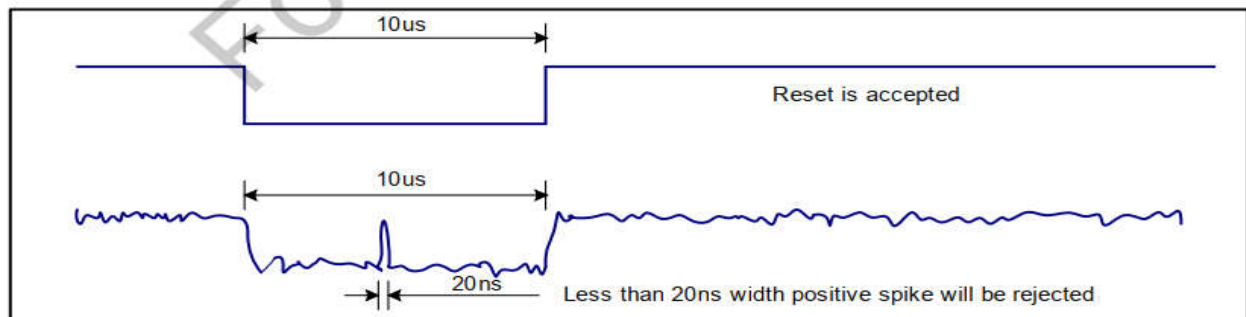
Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset starts in Sleep-out mode. The display remains the blank state in Sleep-in mode) and then return to default condition for H/W reset.

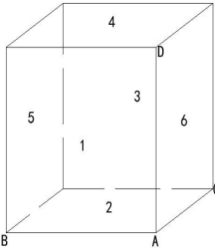
Note 3. During Reset complete time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 10ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 10msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

5.可靠性实验测试(Reliability Test Conditions And Methods)

序号	试验项目	试验条件及方法	试验设备	检验项目	检验工具														
1	高温高湿(静、动态)试验	温度 $60^{\circ}\text{C} \pm 3^{\circ}\text{C}$, 湿度 $90\% \pm 3\%$, 要求选择时间分别为 96 小时, 静、动态(产品点亮)在室温下恢复 2 小时后进行外观, 显示功能检查。	恒温恒湿试验机	检验外观、功能、抗腐蚀性	目视/测试架/客户样机/显微镜														
2	高、低温冲击试验	静态 -30°C (30 分钟) \rightarrow 80°C (30 分钟) \rightarrow -30°C (30 分钟), 24 个循环, 在室温下恢复 2 小时后进行外观, 显示功能检查。	冷热冲击试验机	检验外观、功能															
3	高温贮存试验	常温 $60^{\circ}\text{C} + 3^{\circ}\text{C}$ 、宽温 $70^{\circ}\text{C} + 3^{\circ}\text{C}$ 、96 小时后在室温状态下恢复 1 小时在 2 小时内完成外观、显示功能检查。	烤箱	检验外观、功能	目视/测试架/客户样机														
4	低温贮存试验	常温 $-20^{\circ}\text{C} + 3^{\circ}\text{C}$ 、宽温 $-30^{\circ}\text{C} + 3^{\circ}\text{C}$ 、条件的试验箱内保存 96 小时后在室温状态下恢复 1 小时, 在 2 小时完成外观、显示功能检查, 特别注意检查是否有漏液、断线、腐蚀、偏光片不良现象。	低温冰箱	检验外观、功能															
5	低温贮存试验(动态)	常温 $-20^{\circ}\text{C} + 3^{\circ}\text{C}$ 、宽温 $-30^{\circ}\text{C} + 3^{\circ}\text{C}$ 条件的试验箱内点亮刷屏, 过程中每 1 小时观察一次, 检查显示功能, 如: 异常, 卡机, 花屏等。特别注意检查是否有漏液、断线、腐蚀、偏光片不良现象。	低温冰箱	检验外观、功能	目视/测试架/客户样机														
6	包装模组跌落试验	<p>1、跌落重量及自由落体高度: (图二)</p>  <p>2、自由落体角度如下:</p> <table border="1" data-bbox="284 1545 662 1904"> <thead> <tr> <th>总重量</th> <th>自由落体高度</th> </tr> </thead> <tbody> <tr> <td>0-9kg</td> <td>92cm</td> </tr> <tr> <td>9-25kg</td> <td>76cm</td> </tr> <tr> <td>25-45kg</td> <td>53cm</td> </tr> <tr> <td>45-68kg</td> <td>46cm</td> </tr> <tr> <td>大于 68kg</td> <td>41cm</td> </tr> <tr> <td></td> <td></td> </tr> </tbody> </table> <p>1) 一角: A 角 2) 三菱: A-B, A-D, A-C 3) 六面: 面 1, 面 2, 面 3, 面 4, 面 5, 面 6;</p>	总重量	自由落体高度	0-9kg	92cm	9-25kg	76cm	25-45kg	53cm	45-68kg	46cm	大于 68kg	41cm			包装模组跌落架	测试电性能无异常、外观检验无破损, 无脱离现象	目视/测试架/客户样机
总重量	自由落体高度																		
0-9kg	92cm																		
9-25kg	76cm																		
25-45kg	53cm																		
45-68kg	46cm																		
大于 68kg	41cm																		

7	盐雾试验	标准条件:中性盐雾试验(NSS试验):5%的氯化钠盐水溶液,溶液PH值中性(6.5~7.2),试验温度 $35\pm 2^{\circ}\text{C}$,盐雾的沉降率在 $1\sim 2\text{ml}/80\text{cm}^2.\text{h}$ 之间,时间24h。2.其它特殊要求条件:醋酸盐雾试验(ASS试验):5%氯化钠溶液中配入冰醋酸,溶液PH值为3左右,试验温度 $35\pm 2^{\circ}\text{C}$,盐雾的沉降率在 $1\sim 2\text{ml}/80\text{cm}^2.\text{h}$ 之间,时间24h。	盐雾试验设备	检验外观、功能,盐雾试验结果的判定方法,腐蚀物出现判定法:定性判定,试验后功能测试应OK,外观观察产品无腐蚀现象产生。	目视/测试架/客户样机/显微镜
8	ESD 抗静电试验	测试架测试状态下试验:接触4KV,非接触(空气)8KV放电测试	抗静电枪 (尖头接触放电,圆头空气放电)	检验外观、功能	目视/测试架

6. 光电参数 (Optical Characteristics)

6.1 光学规格 (Optical Specifications)

5 Optical Characteristics

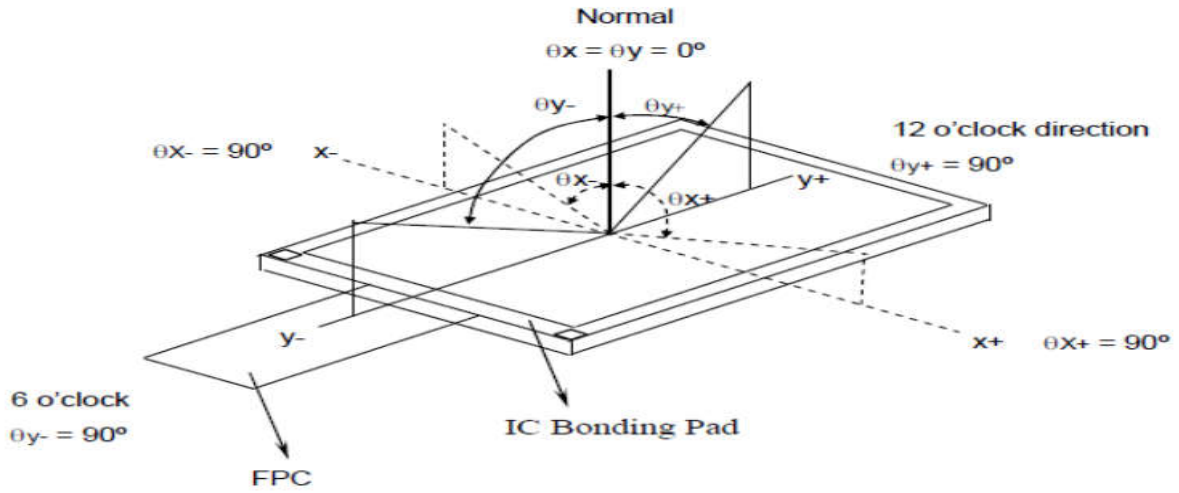
5.1 Optical Specification

EWV Polarizer; Ta=25°C

Item	Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles	θT	Cr≥10	80	85	-	Degree	Note 2
	θB		80	85	-		
	θL		80	85	-		
	θR		80	85	-		
Contrast Ratio	CR	θ=0°	1000	1500	-	-	Note1 Note3
Response time (ms, @ +25C)	Tr+Tf				26	ms	Note1
	GTG				35		Note4
Chromaticity	White	Wx	0.276	0.301	0.326	-	Note5 Note1 Base on LCM
		Wy	0.279	0.304	0.329		
	Red	Rx	0.636	0.656	0.676		
		Ry	0.315	0.335	0.355		
	Green	Gx	0.290	0.310	0.330		
		Gy	0.625	0.645	0.665		
	Blue	Bx	0.133	0.153	0.173		
		By	0.033	0.053	0.073		
NTSC	-	-	78	81	-	%	Note 5
Transmittance	T	-	3.93	4.49		%	Note 1

6.2 视角定义 (Description of View Angle)

Measurement Set Up



7. 检验标准 (Inspection standard)

9.1 Inspection conditions is as follows

- 1) Viewing angle is within $\pm 30^\circ$ from vertical direction, as fig 1
- 2) Viewing angle is the angle defined in the drawing
- 3) Ambient temperature is approximately $25 \pm 5^\circ \text{C}$
- 4) Ambient luminance is about 300~500 Lux.

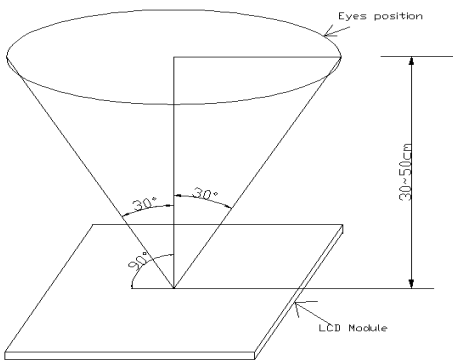
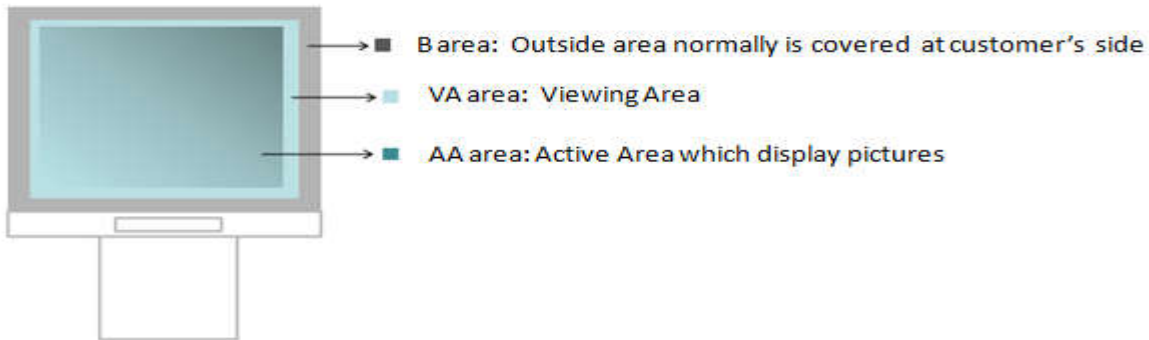
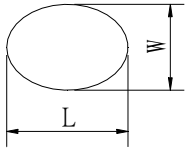


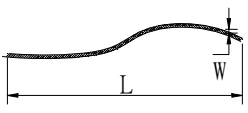
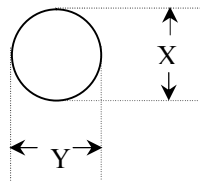
fig1

9.2 Panel area definition



9.3 Routine inspection standards

项目	不良定义	不良现象	判定标准		检验方法			
9.3.1	外观尺寸	与图纸尺寸不相符	NG		卡尺			
9.3.2	功能	显示少线	NG		目视			
		无显示	NG		目视			
		显示异常	NG		目视	主		
		TP 功能不良, 无触摸	NG		目视/用手触摸	主		
9.3.3	点亮产品可见及在 LCD 或 T/P 上有擦拭不掉的点状物	偏光片刺伤、脏点、 圆形物、黑点  $\Phi = (L+W)/2$	LCM/总成 0.95 寸—2.4 寸		目视 (用菲淋卡比对)	次		
			$\Phi \leq 0.10mm$	1、距产品 30mm 目视不见忽略。 2、5mm 间距内只允许 3 个点。 3、显示区只允许 10 个点, 超过以上第 2 第 3 项则 NG。				
				1				
				NG				
			0.15mm < Φ ≤ 0.2mm 按照 A-品入库				LCM/总成 > 2.4 寸——6.0 寸	
			$\Phi \leq 0.10mm$	1、10mm 间距内只允许 3				

				个		
				2、显示区只允许 10 个点，超过以上任意一项则 NG		
			$0.1\text{mm} < \Phi \leq 0.15\text{mm}$	4 (TP、屏各允许 2 个)		
			$0.15\text{mm} < \Phi \leq 0.2\text{mm}$	2 (TP、屏各允许 1 个)		
			$\Phi > 0.2\text{mm}$	NG		
9.3.4	点亮产品可见及在 LCD 或 T/P 上有擦拭不掉的线状物/刮伤		LCM/总成 0.95 寸—6.0 寸	允许个数	目视(用菲琳卡比对)	次
			长(L)	宽(W)		
			$\leq 1\text{mm}$	$\leq 0.03\text{mm}$	2	
			$\leq 2\text{mm}$	$0.03 < W \leq 0.05\text{mm}$	1	
			$> 2\text{mm}$	$> 0.05\text{mm}$	NG	
			两条线毛之间必须距离 5mm 以上 (0.95 寸—3.0 寸). 两条线毛之间必须距离 10mm 以上 (3.1 寸—6.0 寸).			
9.3.5	偏光片气泡	$\Phi = (X+Y) / 2$ 	尺寸	允许个数	在日光台灯下撕起保护膜, 距待测物 30cm 目视	次
			1、 $\Phi \leq 0.1\text{mm}$ 2、不超过边框 1/3	不计 (密集不可)		
			$0.10 < \Phi \leq 0.2\text{mm}$	1		
			$\Phi > 0.2\text{mm}$	NG		
			$0.2 < \Phi \leq 1.5\text{mm}$, (边框以外)	3		
			0.95 寸-2.4 寸气泡间距大于 5mm 以上 > 2.4 寸-6.0 寸气泡间距大于 10mm 以上			
9.3.6	T/P 及偏光片凹凸点	T/P: LCD 偏光片上有凹凸点	可视区有水纹 (擦拭不掉) 拒收 未进入可视区允收, 客户装机后不见允收		在同一视角下用样品比对	次
9.3.7	Mura	边框四周或任一侧的色差、较画面深、区域云状	1.判定画面为 128 灰阶画面, 用 ND filter 盖住 mura 位置进行		ND filter, 128 灰阶	次

		<p>不均、固定位置之图形凹陷状、封口部分较画面深的半圆形、一圈圈均匀的色差、线状 mura、黑画面可见因 spacer 聚集产生的 mura、均匀的实斜线、区域性斜线、Driver IC 与 TFT 匹配问题等原因的 mura</p>	<p>判定。 2、ND1.3 (ND5%可遮盖不见) 3、双方若有签 限度样品, 优先限度样品。</p>	画面	
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